



SEMICON GURUKUL™

Wisdom in Silicon

India's industry-ready VLSI & semiconductor training academy — master the complete chip design flow from RTL to GDSII under working industry experts, with hands-on EDA labs, real industry-grade projects and dedicated placement support.

100%

PLACEMENT ASSISTANCE

Cadence

LICENSED EDA FLOW

24×7

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SCAN TO CHAT

01

FRONT-END VLSI

RTL Design & Functional Verification

The front-end is where a chip's behaviour is born. You translate specifications into synthesizable RTL and prove it works through rigorous functional verification — today's highest-demand skill set in semiconductor design. Starting from digital logic and Verilog fundamentals, you advance to constrained-random, coverage-driven verification: building self-checking UVM testbenches, writing SystemVerilog assertions, and signing off real protocols like AMBA AXI, I2C and SPI on full SoC designs.

TOPICS COVERED

Digital Design Linux TCL-TK Verilog HDL

SystemVerilog (OOP) UVM Methodology

Assertions (SVA) Functional Coverage

AMBA APB/AHB/AXI I2C · SPI

Testbench Architecture Cadence Xcelium

CAREER OUTCOMES

Become an **RTL Design Engineer**, **Design Verification (DV) Engineer** or **SoC Verification Engineer** at firms like Samsung, Synopsys, MediaTek, Intel, Qualcomm, AMD & NVIDIA.

BACK-END VLSI

02

Physical Design & Implementation

The back-end turns logic into silicon. You take a synthesized netlist to a manufacturable GDSII layout on industry-standard **Cadence Innovus** — floorplanning, placement, clock trees, routing and timing closure on real sub-7nm nodes. You'll budget power and IR drop, fix congestion, close timing across corners and modes (MCMM) and clear DRC/LVS signoff — the real flow used to tape out chips.

TOPICS COVERED

CMOS & VLSI Basics Linux · TCL for EDA

Floorplanning Power Planning · IR Drop

Placement · Congestion CTS · Clock Skew

Routing STA · MCMM DRC / LVS Signoff

Cadence Innovus Cadence Tempus

CAREER OUTCOMES

Become a **Physical Design Engineer**, **STA Engineer**, **PnR Engineer** or **Physical Verification Engineer** across India's fast-growing chip-design ecosystem.



SYSTEM MODELLING

SystemC, TLM & Virtual Platforms

Model hardware before RTL even exists. Using SystemC and TLM-2.0 you build SoC virtual platforms that let software teams start months ahead of tapeout — a rare, premium skill valued at every major SoC company. You'll write SystemC modules and TLM transactors, model caches, DMA engines and pipelines, and bring up bare-metal and Linux workloads on RISC-V using QEMU, Spike and Renode — working right at the hardware–software boundary.

TOPICS COVERED

C++ for Hardware SystemC Core

Modules · Processes · Channels TLM-2.0 Sockets

Generic Payload · LT/AT SoC Virtual Platforms

Cache · DMA · Pipeline Models

RISC-V: QEMU · Spike · Renode ARM Fast Models

CAREER OUTCOMES

Become a **SystemC / Virtual Platform Engineer**, **Pre-Silicon Modelling Engineer** or **ESL / Architecture Engineer** at ARM, Intel, NVIDIA, AMD, & Qualcomm.

ARCHITECTURE

RISC-V & GPU Architecture

Go deep into how modern processors and accelerators actually work — from RISC-V instruction encoding and pipeline micro-architecture to GPU SIMT execution and memory hierarchy. You'll design a 5-stage pipeline, handle hazards and branch prediction, explore cache coherence and virtual memory, then dive into GPU warp scheduling, memory coalescing and performance modelling with hands-on profiling labs — the skills that define architecture engineers at the world's top silicon companies.

TOPICS COVERED

RISC-V ISA (RV32I/64) 5-Stage Pipeline · Hazards

Branch Prediction Cache Hierarchy · MESI

Privilege · CSRs · Sv39 VM Custom ISA · RVV Vector

GPU SIMT · Warp Scheduling SM Internals · Memory

Perf Modelling · Nsight

CAREER OUTCOMES

Become a **CPU / GPU Architecture Engineer**, **Performance Modelling Engineer** or **Micro-architecture Engineer** at NVIDIA, ARM, Intel & AMD.



ANALOG LAYOUT

Analog Layout Design

From device physics to silicon-ready layout — this hands-on **Cadence Virtuoso** program covers CMOS fabrication, full-custom standard-cell and analog/mixed-signal layout, matching, layout-dependent effects and clean DRC/LVS signoff, finishing with an industry capstone (BGR, LDO, RDAC).

TOPICS COVERED

Device Physics	CMOS Fabrication	Virtuoso XL
Cell · P-Cell	DRC / ERC / LVS	Parasitic (PEX)
Std-Cell Layout	Device Matching	EM/IR · ESD
Op-Amp · Mirror	LDE Effects	Guard Rings

CAREER OUTCOMES

Become an **Analog Layout Engineer**, **Custom / Mask Layout Engineer** or **Mixed-Signal Layout Engineer** at analog leaders like Texas Instruments, Analog Devices & Qualcomm.

SCRIPTING & AUTOMATION

Linux, Shell, TCL & Python for VLSI

Scripting is the automation backbone of every semiconductor company. Master the Linux environment and the languages engineers use daily to drive EDA tools, automate flows and build utilities — Shell, Perl, TCL/TK and Python. It's the productivity multiplier that sets top VLSI engineers apart and pairs perfectly with any design or layout track.

TOPICS COVERED

Linux Workflows	Shell Scripting	Perl Automation
TCL for EDA Tools	TCL/TK GUIs	Python for VLSI
EDA Flow Automation	Regex & Text Processing	
Makefiles · Version Control		

CAREER OUTCOMES

A high-value add-on for every VLSI role — **Design**, **Verification**, **Physical Design** & **CAD / Flow Engineer** — automation skills that boost productivity and employability.





Course Details & Why Choose Us

Flexible programs · built for engineers · backed by industry

Choose Your Program Duration

2mo

FOUNDATION

Core fundamentals & a single specialised track to fast-track your start.

6mo

PROFESSIONAL

Deeper labs, mini-projects & interview prep for job-ready skills.

9mo

ADVANCED

Full curriculum, daily labs & an industry-standard major project.

Who Can Join

B.Tech / M.Tech students & graduates in **ECE / CSE** and allied electronics branches. No prior VLSI experience needed — we start from the basics with pre-course material.

B.Tech ECE

B.Tech CSE

M.Tech ECE

M.Tech CSE

Final Year

Freshers

What Makes Semicon Gurukul Different

● Trained by Working Engineers

Learn directly from active engineers at top semiconductor companies — real flows, real war stories.

● Industry-Grade Projects & Execution

Work on production-style chip projects run with real-world timelines, design reviews & tape-out-grade sign-off discipline.

● Lab-Oriented, Hands-On Training

Daily hands-on labs that mirror real industry workflows — not toy simulators or slideware.

● Licensed Cadence Toolchain

Train on a genuine, fully-licensed **Cadence** EDA flow with 24/7 cloud lab access.

● 100% Job Placement Support

Dedicated placement cell, mock interviews, resume reviews & direct access to hiring partner companies.

● AI-at-Workplace & Certification

Learn how the industry uses AI and make it your productivity co-pilot — not a threat — plus an industry-recognized certificate.

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